Application No.: 09/990,862 Docket No.: JCLA7288

REMARKS

Present Status of the Application

The Office Action rejected claims 1, 3, 5, 7-8 and 11 under 35 U.S.C. 103(a), as being unpatentable over Patent 6383732 to Hegde et al. Applicants have amended claims 1, 5, 6, 7 and 11 to improve clarity. After entry of the foregoing amendments, claims 1, 3, 5-8 and 11 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The present invention provides a structure of a flash memory, which reduces the amount of variation of the threshold voltage and enhances data retention of the flash memory. The present invention also provides a structure of a flash memory comprising an electron trapping layer, a gate and a source/drain region, wherein the electron trapping layer is formed by stacking in sequence a first oxide layer and a dielectric layer with a high dielectric constant (i.e. a dielectric constant higher than that of Si_3N_4/SiO_2, also known as NO). The dielectric is, for example, Y_2O_3, $HfSi_xO_y$ and Pr_2O_3. The gate is arranged on the electron trapping layer, and the source/drain region is arranged on the substrate of the two lateral sides of the electron trapping layer. In addition, the band gap of the material used for the high dielectric constant dielectric layer determines whether or not a second oxide layer should be provided on the high dielectric constant dielectric layer. The second oxide layer is not needed if the band gap of the high dielectric constant dielectric layer is closer to or greater than that of silicon oxide. On the other

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hand, a second oxide layer is needed if the band gap is smaller than that of silicon oxide. The advantage of the present invention is that a high dielectric constant material is used as the main material for the dielectric layer. Thus, the amount of variation of the threshold voltage is greatly reduced, and data retention of the flash memory is enhanced.

Discussion of Office Action Rejections

The Office Action rejected claims 1 and 7 under 35 U.S.C. 103(a), as being unpatentable over Patent 6,383,732 to Hegde et al.

Applicants respectfully assert that Hegde et al is legally deficient for the purpose of rendering claims 1 and 7 unpatentable for at least the reason that not every element of the claim was taught or suggested by cited references such that the invention as a whole would have been obvious to one of ordinary skill in the art. The present invention specifically teaches "*the dielectric is selected from a group consisting of* Y_2O_3, $HfSi_xO_y$, *and* Pr_2O_3" as taught in claim 1 or "*the dielectric layer having the high dielectric constant is selected from a group consisting of* Y_2O_3, $HfSi_xO_y$ *and* Pr_2O_3". The technical significant of the foregoing limitations is that the dielectric layer of the flash memory is selected from a group consisting of Y_2O_3, $HfSi_xO_y$ *and* Pr_2O_3 to reduce the amount of variation of the threshold voltage and enhance data retention of the flash memory. Hegde et al, on the other hand, discloses a first oxide layer 106 includes a first element and a second element, wherein the first element includes zirconium (Zr), hafnium (Hf), lanthanum (La), niobium (Nb), tantalum (Ta), titanium (Ti) and strontium (Sr), referring to col. 2, line 31-33. Besides, Hegde et al discloses the first oxide layer 106 is a CVD $Zr_xSi_yO_z$ compound,

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referring to col. 3, line 8-9. Hegde et al, however, fails to teach or suggest the claimed features of the present invention. Applicants therefore respectfully submit that Hegde et al does not render the present invention of claims 1 and 7 unpatentable. Applicants respectfully request that the Office withdraw of the rejection of claims 1and 7.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 7 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 3, 5-6, 8 and 11 patently define over the prior art as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1, 3, 5-8 and 11 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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